EIA Low ESR
Multi-Layer Ceramic Capacitors

0402N (0.040” x 0.020”)

Product Features

- High Q
- High Power
- Low ESR/ESL
- Low Noise
- High Self-Resonance
- Ultra Stable Performance
- Capacitance Range: 0.1pF to 33pF
- Working Voltage: 200V

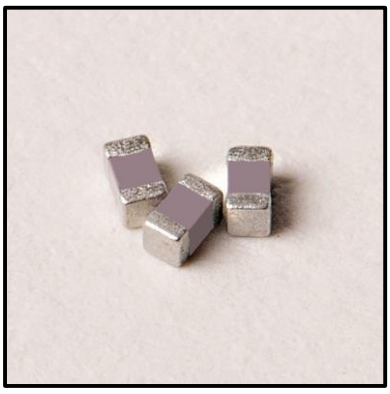
Product Applications

Typical Functional Applications

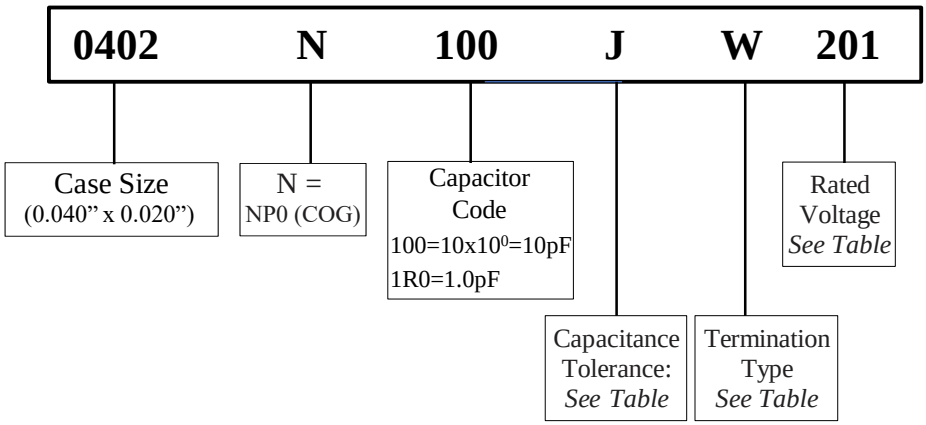
• Tuning • Bypass • Coupling
• Feedback • D.C. Blocking
• Impedance Matching

Typical Circuit Applications

• UHF/Microwave RF Power Amplifiers
• Mixers • Oscillators • Filter Networks
• Low Noise Amplifiers • Timing Circuits and Delay Lines



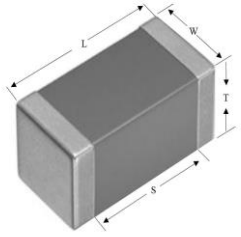
Part Numbering



Capacitor Dimensions

Unit: inch (millimeter)

Code	Term.	Length	Width	Thickness	Overlap
		Lc	Wc	Tc	B
W	Chip	0.040 ± 0.004 (1.02 ± 0.10)	0.020 ± 0.004 (0.51 ±0.10)	0.020 ± 0.004 (0.51 ±0.10)	0.010±0.006 (0.25±0.15)



Capacitance Tolerance Codes

Code	A	B	C	D	F	G	J	K
Tol.	±0.05pF	±0.1pF	±0.25pF	±0.5pF	±1%	±2%	±5%	±10%

EIA Low ESR
Multi-Layer Ceramic Capacitors

0402N (0.040” x 0.020”)

Terminations Type and Code

Termination Code	Termination
W	100% Tin Solder over Nickel Barrier

Voltage Codes

Voltage	Code
50V	500
200V	201
250V	251

0402N Capacitance Values

For special capacitances, tolerances and WVDC, please contact PPI.

Cap. pF	Cap Code	Tol.	Rated WVDC Std.	Rated WVDC Ext.	Cap. pF	Cap Code	Tol.	Rated WVDC Std.	Rated WVDC Ext.	Cap. pF	Cap Code	Tol.	Rated WVDC Std.	Rated WVDC Ext.
0.1	0R1	A,B, C,D	50V or 200V	250V	1.7	1R7	A,B, C,D	50V or 200V	250V	6.8	6R8	A,B, C	50V or 200V	N/A
0.2	0R2				1.8	1R8				7.5	7R5			
0.3	0R3				1.9	1R9				8.2	8R2			
0.4	0R4				2.0	2R0	A,B, C,D	50V or 200V	250V	9.1	9R1			
0.5	0R5				2.1	2R1				10	100	F,G, J,K	50V or 200V	N/A
0.6	0R6				2.2	2R2				11	110			
0.7	0R7				2.4	2R4				12	120			
0.8	0R8				2.7	2R7				13	130			
0.9	0R9				3.0	3R0				15	150			
1.0	1R0				3.3	3R3				16	160			
1.1	1R1				3.6	3R6	A,B, C,D	50V or 200V	N/A	18	180			
1.2	1R2				3.9	3R9				20	200			
1.3	1R3				4.3	4R3				22	220			
1.4	1R4				4.7	4R7				24	240			
1.5	1R5				5.1	5R1				27	270			
1.6	1R6				5.6	5R6				30	300	F,G, J,K	50V	N/A
					6.2	6R2				33	330			

EIA Low ESR
Multi-Layer Ceramic Capacitors

0402N (0.040” x 0.020”)

Electrical Specifications

Quality Factor (Q)	2,000 at 1 MHz min.
Insulation Resistance (IR)	10^5 Megaohms min. @ +25°C rated WVDC 10^4 Megaohms min. @ +125°C rated WVDC
Rated Voltage	See Rated Voltage
Dielectric Withstanding Voltage (WVDC)	250% of Rated Voltage of 5 seconds
Operating Temperature Range	-55°C to 175°C
Temperature Coefficient (TC)	0±30ppm/°C
Capacitance Drift	±0.02% or ±0.02pF, whichever is greater
Piezoelectric Effects	None

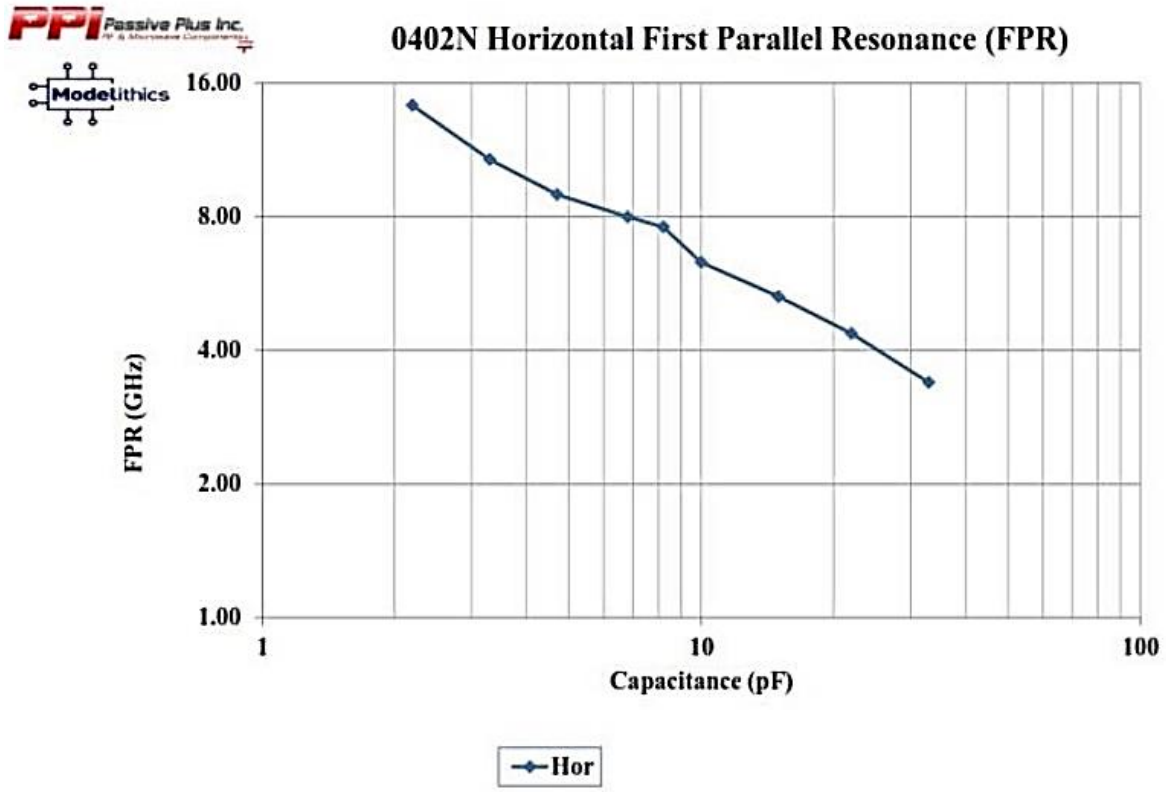
Environmental Specifications

	Specification	Test Parameters
Thermal Shock	No mechanical damage **Capacitance Change:** ±0.5% or 0.5pF max **IR:** >10 G Ohms Q>2000 Breakdown Voltage: 2.5x WVDC	MIL-STD-202, Method 107, Condition A. At the maximum rated temperature (-55°C and 175°C) stay 30 minutes, the time of removing shall not be more than 3 minutes. Perform five cycles.
Humidity (Steady State)	No mechanical damage **Capacitance Change:** ±0.5% or 0.5pF max **IR:** >1 G Ohms Q>300 Breakdown Voltage: 2.5x WVDC	MIL-STD-202, Method 106
Low Voltage Humidity	No mechanical damage **Capacitance Change:** ±0.3% or 0.3pF max **IR:** >1 G Ohms Q>300 Breakdown Voltage: 2.5x WVDC	MIL-STD-202, Method 103, Condition A, with 1.5 Volts DC applied while subjected to an environment of 85°C with 85% relative humidity for 240 hours minimum.
Life	No mechanical damage **Capacitance Change:** ±2.0% or 0.5pF max **IR:** >1 G Ohms Q>500 Breakdown Voltage: 2.5x WVDC	MIL-STD-202, Method 108. For 1000 hours, at 175°C. 200% of Voltage for Capacitors
Terminal Adhesion	Termination should not pull off. Ceramic should remain undamaged	Linear pull force exerted on axial leads soldered to each terminal 2.0lbs.
Resistance to Soldering Heat	No mechanical damage **Capacitance Change:** -1.0%~+2.0% **IR:** >10 G Ohms Q>500 Breakdown Voltage: 2.5x WVDC	Preheat device to 150°C -180°C for 60 seconds. Dip in 260°C ±5°C solder for 10 ±1 second. Measure after 24± 2 hour cooling period.

Capacitors are designed and manufactured to meet the requirements of MIL-PRF-55681 and MIL-PRF-123.

ESR vs. Frequency

First Parallel Resonance



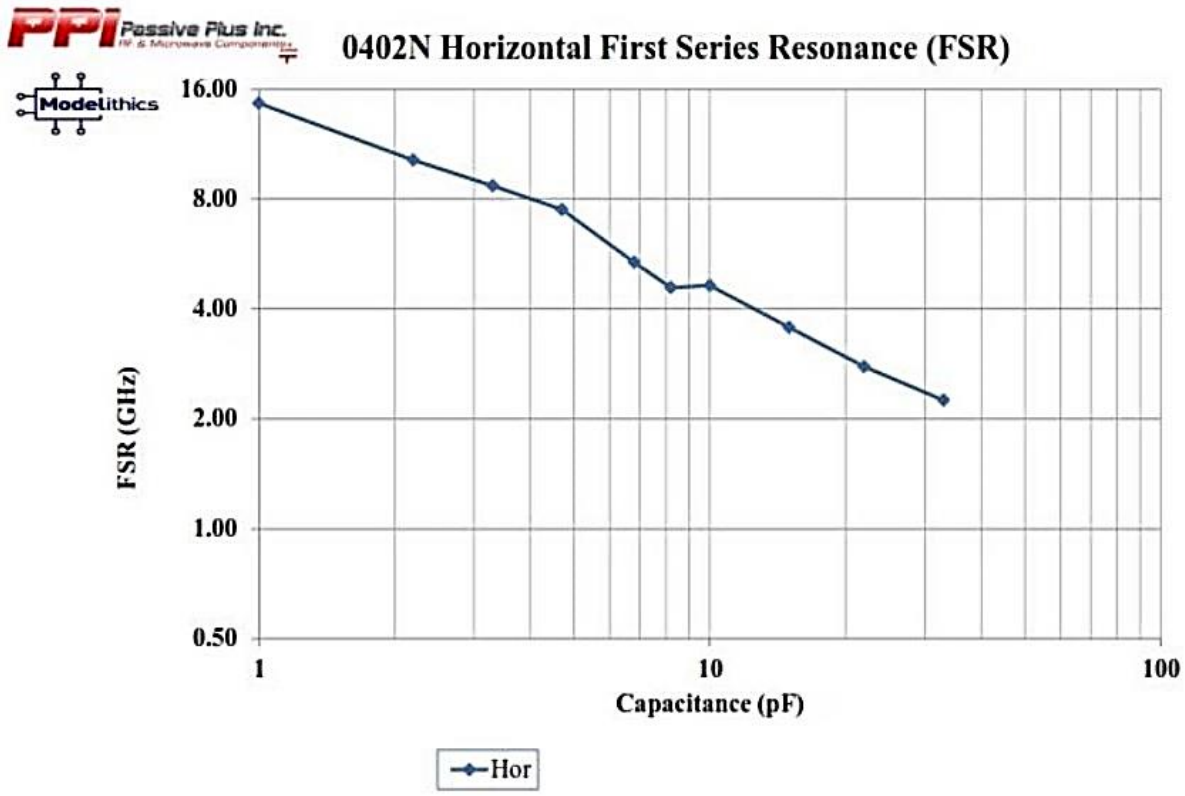
Definitions and Measurement Conditions

The **First Parallel Resonance, FPR,** is defined as the lowest frequency at which a suckout or notch appears in |S21|. It is generally independent of substrate thickness or dielectric constant, but does depend on capacitor orientation. A vertical orientation means the electrode planes are perpendicular to the substrate.

The definitions on the charts are for a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace with 50-Ohm termination. The measurement conditions are: substrate – Rogers RO4350; substrate dielectric constant = 3.48; substrate thickness (mils) = 10; gap in microstrip trace (mils) = 15; microstrip trace width (mils) = 22; Reference planes at sample edges.

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by PPI. The models are derived from measurements on a large number of parts disposed on several different substrates.

First Series Resonance



Definitions and Measurement Conditions

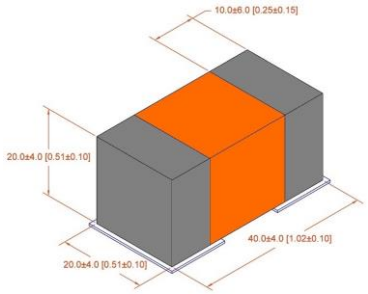
The **First Series Resonance, FSR,** is defined as the lowest frequency at which the imaginary part of the input impedance, Im[Zin], equals zero. Should Im[Zin] or the real part of the input impedance, Re[Zin], not be monotonic with frequency at frequencies lower than those at which Im[Zin] =0, the FSR shall be considered as undefined (represented as a gap in the plot). FSR is dependent on internal capacitor structure; substrate thickness and dielectric constant; capacitor orientation, as defined alongside the FPR plot; and mounting pad dimensions.

The definitions on the charts are for a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace with 50-Ohm termination. The measurement conditions are: substrate – Rogers RO4350; substrate dielectric constant = 3.48; substrate thickness (mils) = 10; gap in microstrip trace (mils) = 15; microstrip trace width (mils) = 22; Reference planes at sample edges.

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by PPI. The models are derived from measurements on a large number of parts disposed on several different substrates.

Capacitor Application Program

Passive Plus, Inc.’s brand new **online Capacitor Application Program (**C.A.P.) helps Engineers and Designers select capacitors according to parameters such as cap value and frequency. C.A.P. allows engineers to insert capacitors requirements (Cap value, Frequency), producing Scattering Matrices (S2P) Charts while providing options (Case Size, Terminations, Mounting), and parameters (ESR, Q, Impedance) along with Datasheets. Once engineers have determined their capacitor requirements, C.A.P. also includes online Requests For Quotes (RFQs) and/or sample requests.



Modelithics Vendor Program

PPI offers design engineers a Free 90-Day Trial license for the Modelithics PPI Component Library. This program provides engineers access to extremely accurate scalable simulation models for Passive Plus capacitors with advanced features that enable a more precise and rapid design process.

Microwave Global Models include every part value in a series and permit users to input substrate thickness, dielectric constant, and loss tangent, as well as mounting pad layout dimensions. Selected models also include capacitor orientation – vertical or horizontal – as an input. Engineers can request FREE use of the models, by either visiting the Passive Plus Resources page (http://passiveplus.com/addldocs_resources.php).

Recommended Land Pattern Dimensions

When mounting the capacitor to substrate, it's important to carefully consider that the amount of solder (size of fillet) used has a direct effect upon the capacitor once it's mounted.

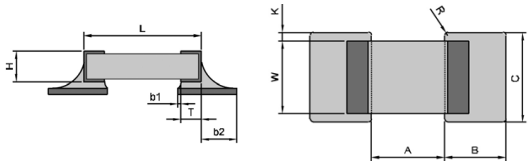
1) The greater the amount of solder, the greater the stress to the elements. This may cause the substrate to break or crack.

2) In the situation where two or more devices are mounted onto a common land, be sure to separate the device into exclusive pads by using soldering resist.

Horizontal Mounting

Dimensions: mm

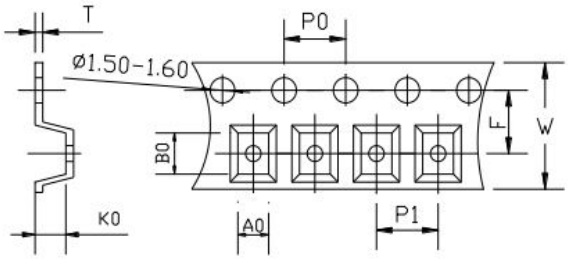
A	B	C
0.3-0.5	0.35-0.45	0.4-0.6



Tape & Reel Specifications

Dimensions: mm

Orientation	Measurement Unit	W	P0	P1	T	F	Minimum Qty per Reel	Std Qty per Reel	Tape Material
H	in.	0.315	0.157	0.079	0.003	0.138	1000	10000	Paper
	mm	8.00	4.00	2.00	0.07	3.50			



$A_0B_0K_0$

- Determined by component size. Typical clearance between the cavity and the component is: .50 (.002) min to .65 (.026) max for 12mm tape.
- The component cannot rotate more than 20° within the determined cavity.

EIA Low ESR
Multi-Layer Ceramic Capacitors

0402N (0.040” x 0.020”)

Engineering Design Kits

PPI offers Design Kits for engineers who are building and testing prototypes. Each kit contains 16 values;10 pieces per value.

Kits are 100% RoHS compliant.

Kit Number	Value Range	Values	
DKD0402N01	**0.1 - 2.0pF**	0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.2, 1.5, 1.6, 1.8, 2.0pF	RoHS
DKD0402N02	**1.0 - 10pF**	1.0, 1.2, 1.5, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2, 10pF	RoHS
DKD0402N03	**10 - 33pF**	10, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33pF	RoHS