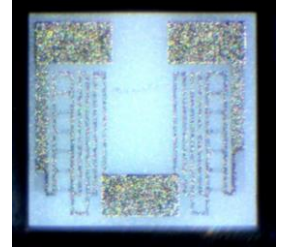




Dual Chip Resistors – PD Series

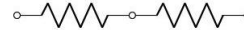
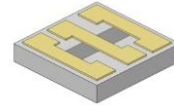
Product Features

- Two resistors on a single chip area.
- Available styles are common or isolated node.
- The nature of this design lends itself to tightly matched TCR and electrical tolerance, with resistance ratios within 0.01% possible (value dependent).
- Can be used in Non-Magnetic Applications

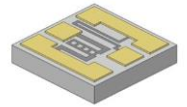


Product Specifications

Resistance Range	2Ω - 1MΩ per resistor (Silicon or Quartz) 2Ω - 160kΩ per resistor (Al ₂ O ₃ , BeO, or AlN)
Resistance Tolerance	±0.01% to ±20% value dependent
Standard Size	30 mil x 30 mil x 10 mil 0.03" x 0.03" x 0.01"

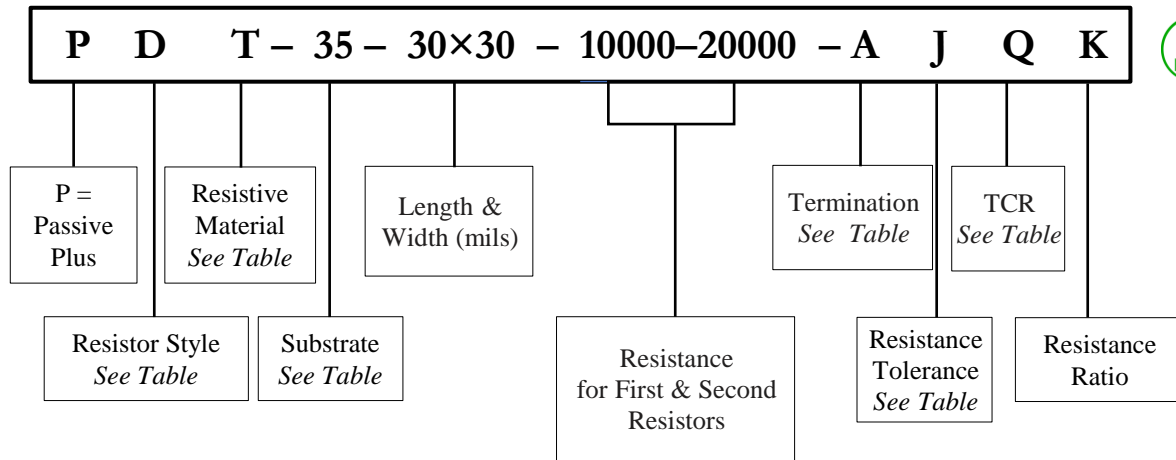


Common Node Configuration



Isolated Node Configuration

Part Numbering



Resistive Style

Code	Style
D	Dual Resistors
I	Isolated Resistors

Resistive Materials

Material	Passivation	Sheet Resistivity (Ω/ Sq)	Abs. Tolerance	Ratio Tolerance
Tantalum Nitride (TaN)	Self Passivating Ta ₂ O ₅	5 to 270	From ±0.01%	From ±0.01%
NiChrome (NiCr)	SiO ₂	5 to 250	From ±0.01%	From ±0.01%

All parts are supplied in waffle packs. Other packaging may be available. Contact PPI for additional packaging options.



Dual Chip Resistors – PD Series

Substrate Materials

Material	Thickness	Surface Finish	Dielectric Constant (@ 1MHz)	Coefficient of Thermal Expansion (x 10 ⁶ /°C)	Thermal Conductivity (W/m*K)	Code	Power per Resistor
Alumina (Al ₂ O ₃)	0.005" - 0.010"	2μ" - 3μ"	9.9	⁷ (25°C to < 300°C)	26.9	35	125 mW
Aluminum Nitride (AlN)	0.005" - 0.010"	6μ" - 8μ"	8.0 - 9.1	^{4.6 - 5.7} (25°C to < 1000°C)	170	28	500 mW
Beryllium Oxide (BeO)	0.005" - 0.010"	< 5μ"	6.76	⁹ (25°C to < 1000°C)	285	25	1 W
Silicon (Si) (with 12kÅ SiO ₂)	0.005" - 0.010"	Chemical Polish	N/A (SiO ₂ K=1.38)	^{2.49 - 4.44} (25°C to < 1000°C)	149 (SiO ₂ 1.38)	22	125 mW
Quartz (Fused Silica)	0.005" - 0.010"	60/40 Optical Polish	3.826	^{0.55} (25°C to < 300°C)	1.38	20	25 mW

Resistance Tolerance Codes

Tolerance	B	D	F	G	H	J	K	L	M	Q	S
Code	± 0.1%	± 0.5%	± 1%	± 2%	± 3%	± 5%	± 10%	± 15%	± 20%	± 0.05%	± 0.01%

Terminations

Metallization		Code
Top Side	Bottom Side	
Pd / Au	—	A
Pd / Au	Ta/Pd/Au	D
Pd / Au	Au Sputtered	K

Temperature Coefficient of Resistance

Material	±150 ppm/°C	±100 ppm/°C	±50 ppm/°C	±25 ppm/°C	±10 ppm/°C	±5 ppm/°C
Tantalum Nitride (TaN)	Q	V	W	X	Y	Z
	Standard	Yes	---	---	---	---
NiChrome (NiCr)	---	---	Yes	Standard	Yes	Yes

Power Handling Range by Material

Case Size mils (inches)	Alumina (C35)	Silicon (C-22)	AlN (C-28)	BeO (C-25)	Quartz (C-20)
30 x 30 (0.030 x 0.030)	125 mW	125 mW	500 mW	1.0 W	25 mW

Resistance Ratio Codes

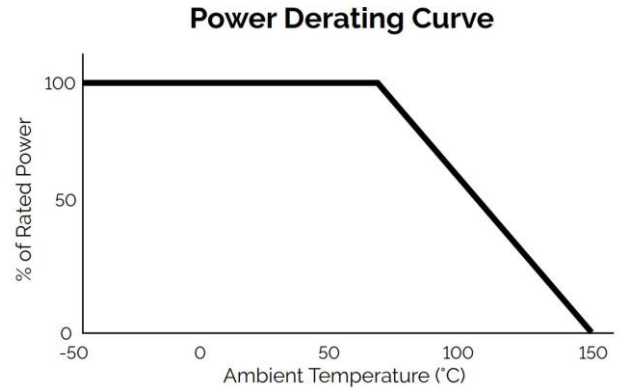
Tolerance To Other Resistors	Code
±0.01%	G
±0.05%	H
±0.10%	J
±0.25%	K
±0.50%	M
±1.00%	N
No Ratio	R



Dual Chip Resistors – PD Series

General Properties

Operating Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Operating Frequency	DC to 500 MHz
Voltage Rating	100V maximum
Power Derating (See Chart at Right)	Full power up to 70°C Derated linearly to zero power at 150°C



Testing

Testing Performed	Specification / Standard
Visual Inspection	MIL-PRF-55342 MIL-STD-883
Mechanical Inspection	MIL-PRF-55342
DC Resistance	MIL-PRF-55342 MIL-STD-202
Resistance Temperature Characteristics (TCR)	MIL-PRF-55342
Short Time Overload	MIL-PRF-55342
High Temperature Exposure	MIL-PRF-55342
Thermal Shock	MIL-PRF-55342 MIL-STD-202
Resistance to Bonding Exposure	MIL-PRF-55342
Wire Bonding Integrity	MIL-PRF-55342
Life Test	MIL-PRF-55342 MIL-STD-202

Performance Specifications

Higher power ratings, additional sizes, and custom resistors available. Please contact sales@passiveplus.com.

Packaging

ESD waffle packs are standard. Film rings and gel pack packaging are available upon request.

